FIG.1

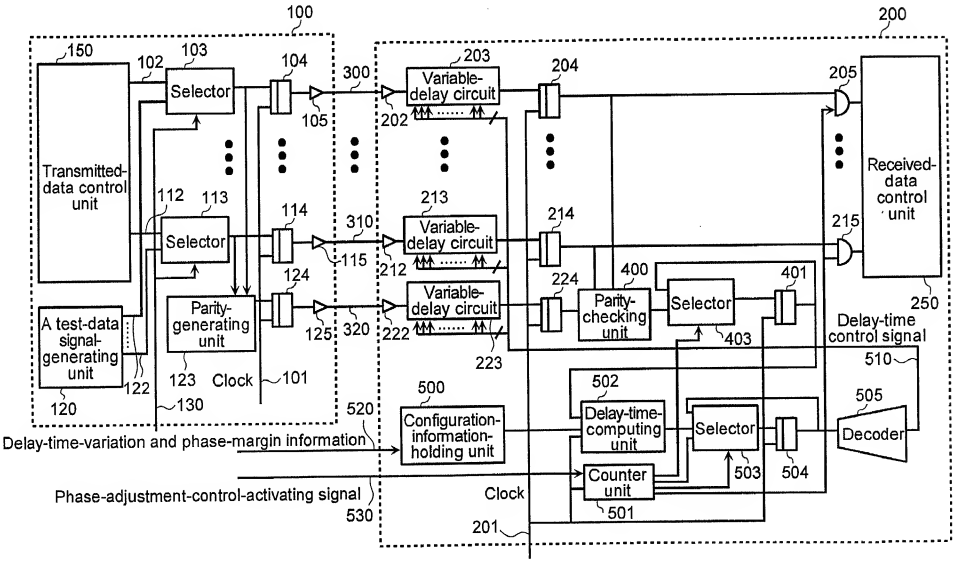
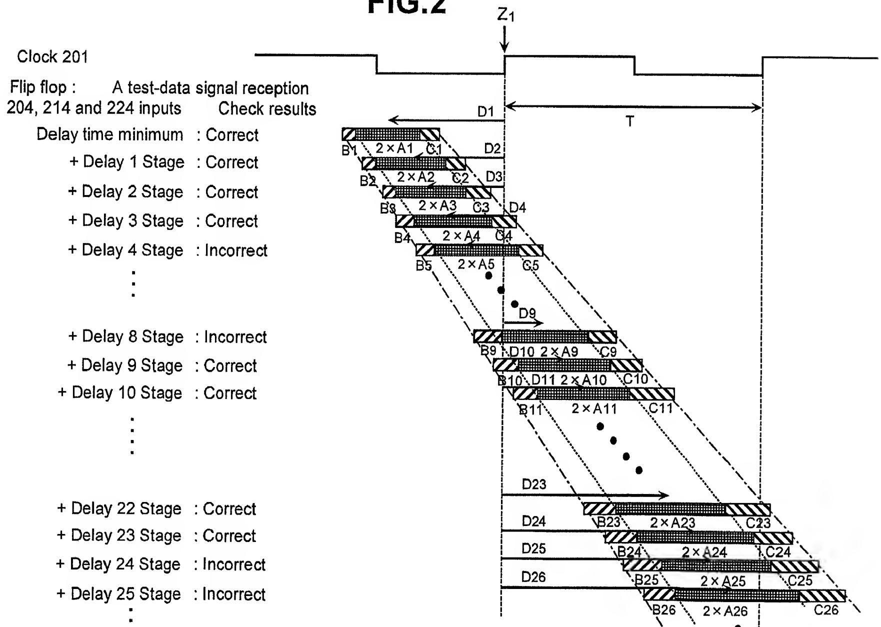
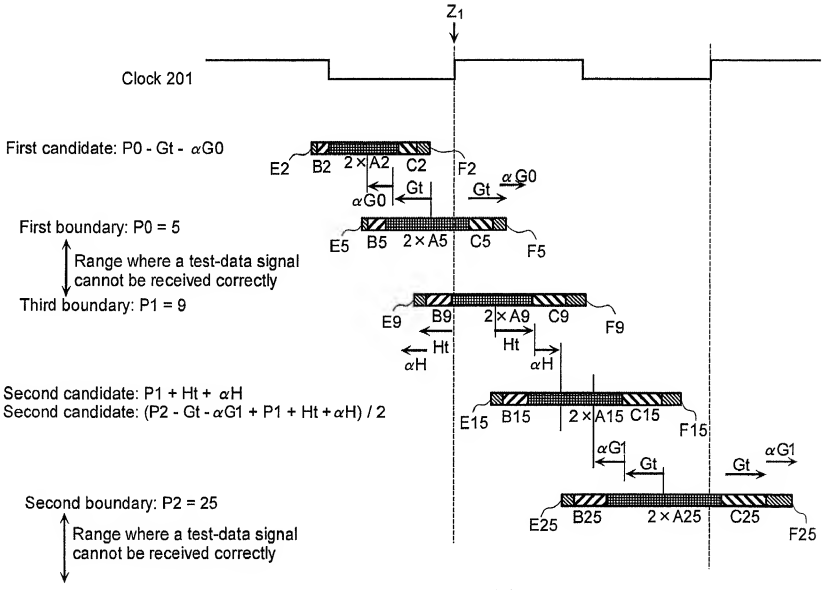

100
200
150
102
103
104
300
203
204
205
Transmitted-data control unit
Selector
Variable-delay circuit
Received-data control unit
105
202
112
113
114
310
213
214
215
Selector
Variable-delay circuit
115
212
124
224
400
401
250
Parity-checking unit
Selector
A test-data signal-generating unit
Parity-generating unit
Variable-delay circuit
Delay-time control signal
125
320
222
223
403
510
122
123
Clock
101
502
505
120
130
500
Delay-time-computing unit
Selector
Decoder
520
Configuration-information-holding unit
Delay-time-variation and phase-margin information
Counter unit
503
504
Phase-adjustment-control-activating signal
530
Clock
501
201

FIG.2



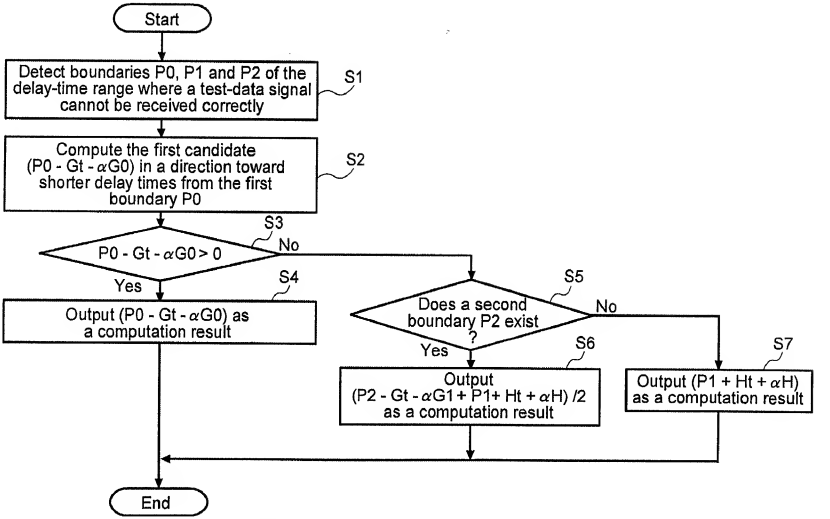
Phase relations between received-data indeterminate times and a clock signal

FIG.3



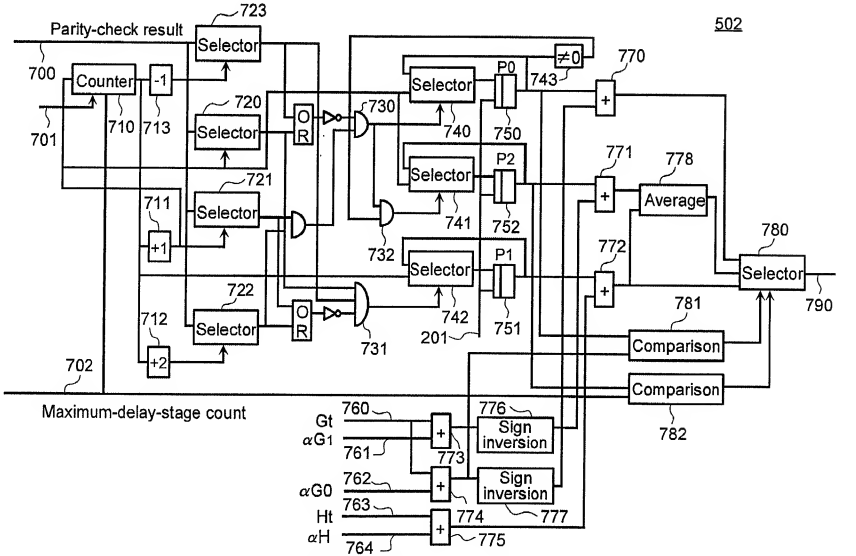
Relations between delay-time variations, external set information and computed delay times

FIG.4



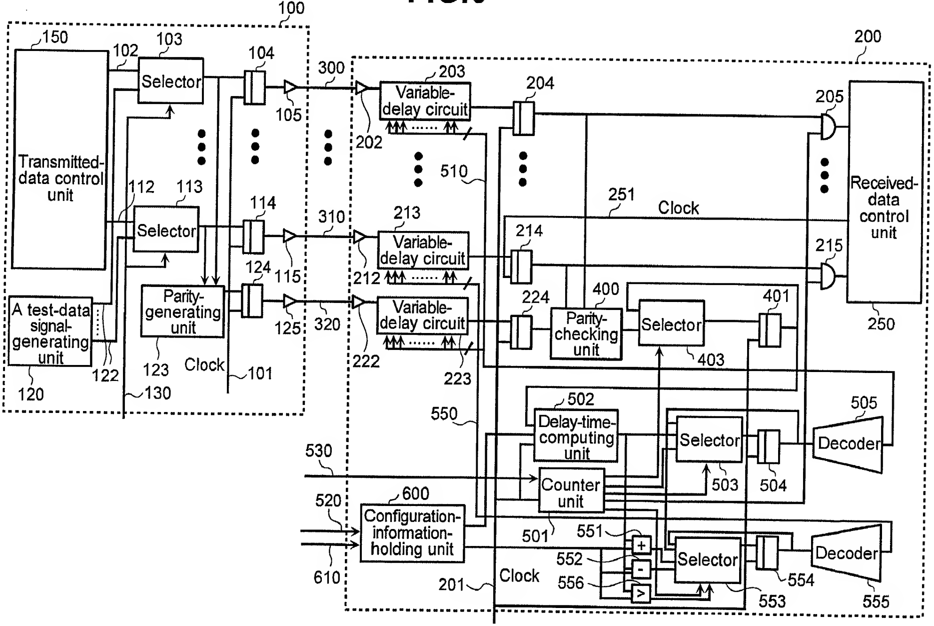
Algorithm of the delay-time computation

FIG.5



Typical circuit configuration of delay-time-computing unit

FIG.6



100
150
Transmitted-data control unit
102
103
Selector
104
105
112
113
Selector
114
115
124
125
A test-data signal-generating unit
120
122
Parity-generating unit
123
Clock
101
130
300
310
320
200
203
Variable-delay circuit
202
213
Variable-delay circuit
212
Variable-delay circuit
222
223
510
550
204
214
224
205
215
Received-data control unit
250
251
Clock
400
Parity-checking unit
Selector
403
401
502
Delay-time-computing unit
Counter unit
501
Selector
503
504
Decoder
505
551
552
556
Selector
553
554
Decoder
555
530
520
610
600
Configuration-information-holding unit
201
Clock

FIG.7

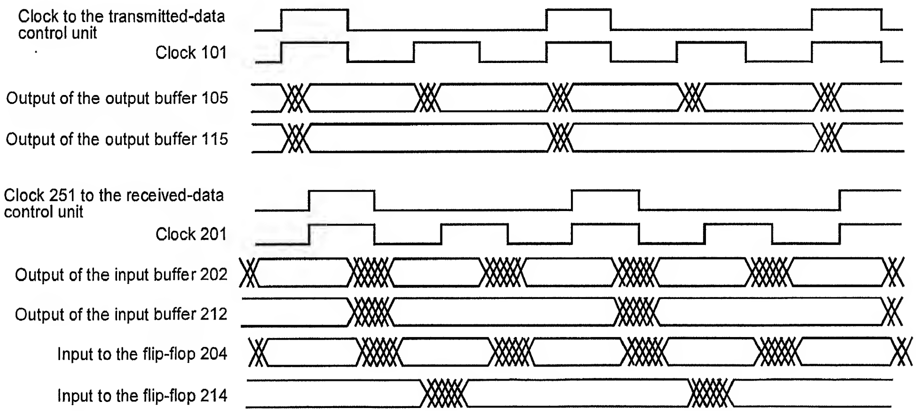

Clock to the transmitted-data control unit
Clock 101
Output of the output buffer 105
Output of the output buffer 115
Clock 251 to the received-data control unit
Clock 201
Output of the input buffer 202
Output of the input buffer 212
Input to the flip-flop 204
Input to the flip-flop 214

FIG.8

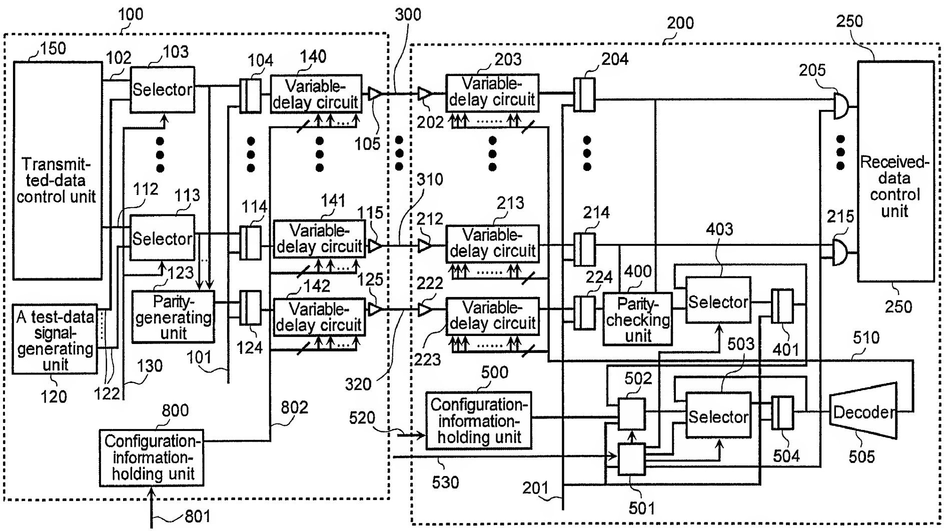
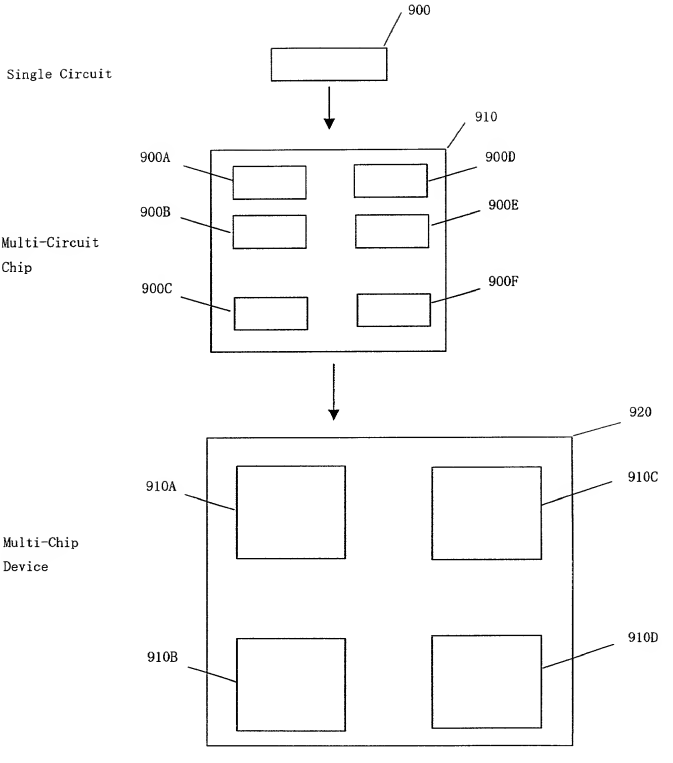

100
150
Transmit-ted-data control unit
102
103
Selector
104
140
Variable-delay circuit
105
112
113
Selector
114
141
Variable-delay circuit
115
123
Parity-generating unit
142
Variable-delay circuit
125
124
A test-data signal-generating unit
120
122
130
101
800
Configuration-information-holding unit
801
802
300
310
320
200
203
Variable-delay circuit
202
204
212
213
Variable-delay circuit
214
222
Variable-delay circuit
223
224
400
Parity-checking unit
403
Selector
401
205
215
250
Received-data control unit
500
Configuration-information-holding unit
520
530
201
502
501
503
Selector
504
510
Decoder
505

Fig. 9


900
Single Circuit
910
900A
900D
900B
900E
Multi-Circuit
Chip
900C
900F
920
910A
910C
Multi-Chip
Device
910B
910D